A stability algorithm for high-level QAM carrier recovery

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Abstract—This paper proposes a structure of the joint frequency-phase carrier recovery loop for all-digital Quadrature Amplitude Modulation (QAM) receivers. The steady-state estimation variance is greatly reduced by introducing a non-zero-mean input to the Stop-and-Go controller. It has been verified by simulation tools that the circuit can acquire frequency offset up to 6% of the symbol rate and phase offset up to 30 degree in only 11000 symbol periods, while its steady-state phase jitter also significantly reduces to 0.11 degrees.

Keywords—Quadrature Amplitude Modulation; carrier recovery; frequency detection; phase detection; stability algorithm

I. INTRODUCTION

The Quadrature Amplitude Modulation (QAM) plays an important role in the broadband communication systems, at the same time, in satellite communications systems, high-order QAM will occupy a great advantage due to its high spectral efficiency in the future.\[1\] - [2].

The carrier recovery performance is an important part in input systems, which requires a very small steady-state phase jitter. Traditionally, the blind carrier recovery is accomplished by various phase-locked loop (PLL) algorithms[3]-[4]. Unfortunately, PLL methods require residual frequency errors much less than the symbol rate; Otherwise, the frequency required to capture approaches such as FPD method [5] - [7], and frequency estimation [8], which require complex and a huge extra cost. On the other hand, the smaller error jitter of the modulator is also essential. As the PLL method is originally designed for the low-level QAM, therefore, its performance will be greatly diminished for the higher-order QAM.

In this article, we introduce the QAM signals to frequency detection (FD) firstly, and then put forward a combination of all-digital carrier frequency of the phase recovery methods, so it is not only the completion of phase retrieval, but also be able to complete clock recovery. Further more, the structure is simple. This method of lowering jitter can significantly improve the performance of high-order QAM when receiving system steady-state. It is better than the DD algorithm with steady-state phase jitter.

II. MATHEMATICAL MODEL

Considering an M-state QAM signal transmitted over an additive white Gaussian noise (AWGN) channel, the signal demodulates to the baseband signal of $r(t)$ with the local oscillator frequency $\omega_0$ and the initial phase $\theta_0$. Denoting the carrier frequency offset and initial phase offset between transmitter and receiver as $\Delta \omega = \omega - \omega_0$ and $\Delta \theta = \theta - \theta_0$.

$$r(t) = \sum_d g(t - kT) \sum \left\{ e^{j(\omega_0 kT + \omega kT + \Delta \omega)} + N(t) \right\}$$

(1)

Where $N(t)$ is a noise component, $g(t)$ is the transmit filter impulse response, $T$ is the symbol interval, $\omega$ is the fractional symbol time shift, $d$ is the sequence of transmitted QAM symbols. The carrier recovery aims at estimating and compensating both $\Delta \omega$ and $\Delta \theta$ on the baseband samples. Assume the clock synchronization is perfect so that the phase offset can denote that

$$\psi_k = \Delta \omega (kT + \omega kT) + \Delta \theta$$

(2)

In order to solve opposite sign of two consecutive phase offset on the edge of the sentence, frequency error signal is expressed as (just like stop-and-go method):

$$e_k = \begin{cases} \psi_k - \psi_{k-1} & \text{sgn}(\psi_k) = \text{sgn}(\psi_{k-1}) \\ e_{k-1} & \text{sgn}(\psi_k) \neq \text{sgn}(\psi_{k-1}) \end{cases}$$

(3)

Where $\text{sgn}(x)$ is the signum function for variable $x$, the signal of $r(t)$ can be used to estimate the phase offset $\psi_k$ in generally:

$$\hat{\psi}_k = \arctan\left(\frac{\text{Im}(r_k)}{\text{Re}(r_k)}\right)$$

(4)

However, in a stable state since $E(\psi_k') = 0$, $E(e_k) = 0$ can be easily changed their sign, it will lead to large jitter.

To ensure the stationarity of jitter, we can replace $\hat{\psi}_k$ with $\hat{\psi}_k = \hat{\phi}_k + c \sum_{i=1}^{k} \hat{\psi}_i$ , the result will be

$$E_k = \begin{cases} \hat{\alpha}_k - \hat{\psi}_{k-1} & \text{sgn}(\hat{\alpha}_k) \neq \text{sgn}(\hat{\alpha}_{k-1}) \\ E_{k-1} & \text{sgn}(\hat{\alpha}_k) = \text{sgn}(\hat{\alpha}_{k-1}) \\ \end{cases}$$

$$e_k + c \hat{\psi}_k \text{sgn}(\hat{\alpha}_k) \neq \text{sgn}(\hat{\alpha}_{k-1})$$

$$E_{k-1} \text{sgn}(\hat{\alpha}_k) = \text{sgn}(\hat{\alpha}_{k-1})$$

(5)

Where $c$ is the anti-jitter factor, the introduction of $c$ can be taken into account as the initial phase error, on the other
hand, $E(\hat{\alpha}_r) \neq 0$, the carrier error signal will be almost without any change in the nature of their symbols in the noisy state, as showed by circuit structure of Figure 2. Therefore, the error will be greatly reduced, and steady state error curve is much smoother so that its performance has been greatly improved.

III. THE CARRIER RECOVERY CIRCUIT STRUCTURE

People usually use the DD algorithm to detect the frequency of the sentence, but since the signal $I_z$ is closely linked to $Q_z$, if $I$ and $Q$ signal frequency offset and phase offset signals are so great that judgment of $I_z$ and $Q_z$ will make an error, DD algorithm will become invalid. In the high-order QAM systems, the above is particularly vulnerable.

Therefore, the literature [9] has made some improvement on the basis of the circuit of Kim and Choi. Circuit takes frequency discriminator phase detector and the combination of the two algorithms structural form. When confronting a large frequency deviation, it uses frequency discriminator (FD).

When the frequency offset and phase error is small, it can be switched to the DD algorithm by the lock detector control, which is using improved phase detector (PD). Whether on the FD or PD working condition, the loop filter gain can be dynamically adjusted to meet the loop capture range and phase tracking jitter of the different needs of two groups, which can be set to gain value. Firstly using a larger loop gain can obtain a faster capture speeds and larger capture range, and then captured by using a smaller loop gain leads to the smaller phase jitter.

However, when compared with the DD algorithm, the steady-state phase jitter increases, and its complexity is still relatively large. This paper based on the paper [8] [9] proposes a new structure as shown in Figure 1, and will use a modified DD algorithm before joining the steady-state phase jitter factor so that the steady-state jitter can be reduced. Combined with large offset FD can improve its performance, and reduces its complexity greatly.

The phase detector of Figure 1 uses anti-jitter decision-directed algorithm (DD algorithm). In particular, by adding the anti-jitter factor in steady state, the lock detector combines with the polarity of Discriminator Sentencing Law, which can increase the stability of the circuit after the stable performance.

The proposed carrier recovery circuit is the traditional structure of other modules, so shall not repeat.

IV. SIMULATIONS RESULTS

To verify the feasibility of the method, we simulate the system by using MATLAB software, and set the carrier recovery loop symbol rate as $F_s (6.016MHz)$. The output of loop filter integral slip is the loop of error available Convergence (offset catch) simulation curve (16QAM mode) in simulation environment. The simulation result is shown below that the circuit can correct the frequency offset value in 0.06Fs and 30 ° of phase shift.

The steady-state phase jitter performance can be presented in Figures 3a, b when Signal to Noise Ratio (SNR) is 12dB and 18dB respectively. We can see the loop stability...
with anti-jitter factor is greatly improved and as the correct frequency offset increases, the steady-state phase jitter performance become no worse.

![Figure 4a. without anti-jitter factor](image1)

(a) without anti-jitter factor

![Figure 4b. with anti-jitter factor](image2)

(b) with anti-jitter factor

Figure 4. capture curves SNR=12dB $\Delta \omega_T = 0.06$

Figures 4a, b can be captured by the offset curve, when using and without using anti-jitter circuit structure respectively, when SNR are 12dB. Figures 4a, b in the offset for the signal are 0.06 Fs, so vertical axis take the normalized frequency offset value and the number of horizontal symbols per sample, in which $C$ is 0.1.

Observing in Figure 4a 15000 ~ 20000 symbol samples within the curve, we can found that the curve is very severe jitter without additional anti-jitter factor of circuit polarity decision phase detection algorithm in 10000 after the full capture offset symbol sampling. Figure 4b is the proposed capture of anti-jitter circuit simulation curve offset. Lock detector will switch the frequency detector to the phase detector between the two operating modes. Though the number of captured symbols slightly enlarges a little, the curve of the jitter with anti-jitter factor will be more regulation, and thus makes the whole curve of the jitter amplitude reduced. Its steady-state phase jitter also significantly reduces to 0.11 degrees.

![Figure 5. The 16-QAM symbol rate error curve $\Delta \omega_T = 0.06$](image3)

Figure 5. The 16-QAM symbol rate error curve $\Delta \omega_T = 0.06$

When there is 6% of the symbol rate frequency shift, 16QAM, the BER of the theoretical values and simulation values are compared, while Carrier recovery using this method is shown in Figure 5. The results show that when the bit error rate $10^{-4}$, the demodulator loss of about 1.7 dB.

Figure 6 show the 64QAM constellation diagram when the frequency offset is 0.06 Fs, SNR = 12 dB. Figure 7 shows the circuit obtained by applying the final correction effect.

![Figure 6. $\Delta \omega_T = 0.06$ SNR=12dB 64QAM constellation](image4)

Figure 6. $\Delta \omega_T = 0.06$ SNR=12dB 64QAM constellation

![Figure 7. Constellation after carrier recovery](image5)

Figure 7. Constellation after carrier recovery

V. CONCLUSION

This paper designs an anti-jitter for QAM carrier recovery circuit. On the one hand, with the use of factors with anti-shake, DD algorithm greatly reduces the impact of the value of constellation points on the phase jitter model and increase the steady-state performance; on the other hand, by timely switching loop lock detector algorithm, it can ensure the advantages of combining the two algorithms and can improve the convergence rate of the loop relatively to other algorithms. The carrier recovery circuit can capture 0.06Fs of the frequency offset and phase offset in only 11000 symbol period when SNR are 12dB, which has great performance advantages relative to the existing circuit.


