A Novel BIST Scheme for Low Power Testing

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Abstract—A novel BIST structure is presented which can greatly reduce the test power dissipation without losing fault coverage. Single input change test pattern is generated by a counter and a gray encoder. The built-in test vectors are generated by the single input change patterns which are exclusive-ORed with seeds generated by the modified LFSR. All test vectors will be single input change patterns during 2^n test clock period. Thus the switching activities of test vectors are greatly reduced in test mode without compromising fault coverage. The proposed structure has the advantages of low test power and low hardware overhead. Experiments conducted on ISCAS'89 benchmark circuits demonstrate that proposed scheme gives better fault coverage with a large reduction in power dissipation during testing.

Keywords—build-in self test; single input pattern testing; low power; switching activity.

I. INTRODUCTION

Power consumption in test mode is usually higher than that in normal mode, and it has been shown that power consumption during test mode is as high as 200% of the power consumed in the normal mode [1]. In general, the test power issues include excess average and excess peak power. The excess average power consumption will result in high accumulated heat, and the excess peak power consumption can cause some reliability problems or even damage the circuit under test. The main reason is that the circuit under test has much more switching activities. Thus special care must be taken to ensure that the power rating of circuits is not exceeded during test application. A number of techniques to control power consumption in test mode have been presented in the literature. These include test scheduling algorithms under power constraints, techniques for minimizing power during scan testing, and low-power built-in self-test (BIST).

Embedded logic blocks used in VLSI chips usually have low controllability and observability. BIST structures are well-suited for testing such blocks. Also, the use of efficient BIST structures allows at-speed testing, can provide very high fault coverage and brings down the cost of testing [2]. BIST also supports test reuse and protects intellectual property [3]. Because of well known characteristic, BIST has been widely studied and applied. However, there are some major drawbacks for this BIST whose architecture is based on the linear feedback shift register (LFSR). One is that the BIST circuit introduces more switching activities in the circuit under test during test than that during normal operation [4]. That can cause excessive power dissipation, and results in delay penalty into the design [5]. To lower the power in test mode, many techniques have been proposed to reduce the switching activities of test pattern. For LFSR based test pattern generator (TPG), Guiller proposed a modified clock scheme for linear feedback shift register (LFSR), so that only half of the D flip-flops works during each test period, thus only half of the test pattern can be switched [6]. DS-LFSR is proposed in [7], in which there’s d times clock frequency between slow LFSR and normal LFSR, and test pattern generated by original LFSR is rearranged to reduce the switch frequency. LP-TPG is proposed by [8]. These techniques can efficiently reduce the average power compared to traditional pseudo random BIST circuits, but sometimes lead to fault coverage reduction.

Single input change sequence technique is a better low power approach which greatly decreases the transitions of inputs to reduce the internal switching activities. In [2], [4], and [9-11], the combination of LFSR and scan shift registers is used to generate random single input change sequences. In [4] and [11], a pseudo single input change sequence technique is proposed by adding an extra cyclic shift register and XOR gates, so that 2n-1 single input change test vectors can be inserted between two neighbor vectors generated by LFSR, n is the length of LFSR. Thus average power is reduced. The drawback of this methodology is that the test vectors’ switching activities will still be very large if the test clock frequency is very high since the seed changes every 2^n clock period.

In this paper, we present a novel BIST scheme which generates more efficient single input change test patterns. The single input changing generator (SICG) includes an n-bit counter and n-bit gray encoder. 2^n continuous n-bit binary data is generated by an n-bit counter, encoded by a gray encoder, and 2^n single input changing data are generated. Then the single input changing data is exclusive-ORed with the seed generated by modified LFSR. For the n-bit modified LFSR, the largest non-related random data number is 2^n-1, where 2^n single input changing data is inserted between two neighboring seeds, thus 2^n * (2^n-1) single input changing test vectors can be generated. In this scheme, the seed generated by the modified LFSR will be changed every 2^n (m<=n) clock period, so it is very suitable for BIST in very large scale sequential circuits, especially SoC.

The rest of the paper is organized as follows. Section II gives an overview of test power analysis. Section III presents the proposed BIST architecture. Section IV describes experimental results. Section V summarizes the paper.
II. TEST POWER ANALYSIS

There are four power consumption sources in CMOS process: leakage current power consumption, direct-path short circuit current power consumption, standby current power and switching current power. The leakage current power consumption is primarily determined by fabrication technology considerations. Direct-path short circuit current arises when both the NMOS and PMOS transistors are simultaneously active and conducting current directly from supply to ground. As the dominant part in a well-designed circuit is the switching current power consumption, to minimize the switching power is critical for low power design. For scan-based CUT, there are mainly two factors contributing to the switching power. One is the switching activities in the combinational logic, the other is the shifting activities between scan cells [4]. The parameters related to power consumption are the electric energy consumption \( E_i \) during a period and average power consumption \( P_i \) of internal circuit node \( i \).

The electric energy consumption \( E_i \) [13] can be given in the following equation:

\[
E_i = \frac{1}{2} V_{dd}^2 C_0 F_i S_i \quad (1)
\]

Where \( V_{dd} \) is the supply voltage, \( C_0 \) is the loading capacitance, \( F_i \) is the fan-out number, \( S_i \) is the switching times during the period. The total energy consumption is the power accumulation \( E_i \) of all internal nodes.

Average power consumption of node \( i \) can be given by:

\[
P_i = \frac{1}{2} V_{dd}^2 C_0 F_i S_i / f \quad (2)
\]

Where \( S_i \) is the average switching times during the period. \( f \) is the clock frequency. The average power consumption is the summary of \( P_i \) of all nodes.

From (1) and (2), it can be easily found that the energy and power consumption depends on the switching activities for a fixed circuit structure, voltage and fixed clock frequency. The switching activities can be reduced by inserting \( 2^m \) vectors between two neighboring seeds, in which each vector has only one bit difference with the last vector, thus pseudorandom single input changing vectors are generated.

III. PROPOSED BIST ARCHITECTURE

LFSR is widely used as test pattern generator because of its small circuit area and excellent random characteristics. Modified LFSR is used as the seed generator in this paper. As shown in Fig. 1, the proposed architecture which is called LSA-TPG consists of a seed generator (SG), an n-bit counter, a gray encoder and an exclusive-OR array. The n-bit counter and gray encoder generate single input changing patterns. C[n-1:0] is the counter output and G[n-1:0] is the gray encoder output. The counter and SG are controlled by test clock TCK. The initial value of the n-bit counter is all zeroes, and it generates \( 2^n \) continuous binary data periodically. The output of NOR operation of C[n-1:0] will be the clock control signal of SG where \( m \leq n \). It can be found obviously that SG will generate the next seed only when C[m-1:0] are all ‘0’ and NOR output changes to ‘1’. The period of the single input changing sequences will be \( 2^m \).

![Figure 1. Structure of low power test pattern generator (LSA-TPG).](image)

Gray encoder in Fig. 1 is used to encode the counter’s output C[n-1:0] so that two successive values of its output G[n-1:0] will differ in only one bit. Gray encoder can be implemented by following equations.

\[
G[0] = C[0] \text{ XOR } C[1]
\]
\[
\]
\[
\]
\[
\vdots
\]
\[
G[n-2] = C[n-2] \text{ XOR } C[n-1]
\]
\[
G[n-1] = C[n-1]
\]

The seed generating circuit SG is a modified LFSR which is the combination of a Type I LFSR and several XOR gates. The theory in [12] stated that the conventional LFSR’s outputs can not be taken as the seed directly, because some seeds may share the same vectors. So the seed generator circuit should make sure that any two of the signal input changing sequences do not share the same vectors or share as few vectors as possible. The final test patterns are implemented as following equations.

\[
V[0] = S[0] \text{ XOR } G[0]
\]
\[
\]
\[
\]
\[
\vdots
\]
\[
V[n-1] = S[n-1] \text{ XOR } G[n-1]
\]

The SG’s clock will be TCK/2^m due to the control signal. As SICG’s cyclic sequences are single input changing patterns, the XOR result of the sequences and a certain vector must be a single input changing sequence too.

Fig. 2 is an example of counter and gray encoder’s output when \( n=4 \) and \( m=3 \). The seed does not change in a cycle when \( C[2:0] \neq \text{ "000" } \), and it will only switch to another vector when \( C[2:0] = \text{ "000" } \). It can be found that all values of G[3:0] are single input changing patterns.
Fig. 2. An example of gray encoder output (n=4).

Fig. 3 is an example of 4 bit single input changing sequence with the seed S0 “0000” and with the seed S1 “0101” when n=4 and m=3. The period of the single input changing sequences will be 8. 4-bit gray encoder output sequence in Fig. 3 is {0000, 0001, 0011, 0010, 0110, 0111, … 1000}. The chosen seeds S0 and S1 are {0000} and {0101}. S0 will be exclusive-ORed with sequence {0000, 0001, 0011, … 0100} and generates the SICG single input changing sequence {0000, 0001, 0011, 0010, 0110, 0111, 0101, 0100}, S1 will be exclusive-ORed with sequence {1100, 1101, 1111, …1000} and generates the SICG single input changing sequence {1001, 1000, 1010, 1011, 1111, 1110, 1100, 1101}. As an example, two well chosen seeds guarantee two single input changing sequences are unique.

S0=0000 S1=0101
V0 =0000 V8 =1001 V1 =0001 V9 =1000 V2 =0011 V10 =1010 V3 =0010 V11 =1011 V4 =0110 V12 =1111 V5 =0111 V13 =1110 V6 =0101 V14 =1100 V7 =0100 V15 =1101

Fig. 3. An example of 4 bit single input changing sequence (n=4,m=3).

Fig. 4 is the circuit structure of single input changing generator (SICG).

The SICG circuit in Fig. 4 consists of an n-bit counter and a gray code encoder. The n-bit counter consists of n D flip-flops and the gray encoder consists of n-1 exclusive-OR gates. So the hardware overhead can be controlled under reasonable scope and the power consumption can be greatly reduced while the fault coverage is guaranteed. It is applicable for large scale circuits especially for SoC.

IV. EXPERIMENTAL RESULTS

To validate the effectiveness of the proposed approach, we select traditional LFSR technique for comparison. Experiments on ISCAS ’89 benchmark circuits were conducted. Simulations and analysis were carried out with Synopsys Design Compiler, Primepower and Hspice. Test application and test response were taken during every clock period. TSMC 0.13 µm CMOS library is used. The test frequency is 1 GHz and the power supply is 1.5 V.

A. Power Consumption Comparison

Table I shows the comparison of experimental results of the average test power consumption with the traditional LFSR method, and with the proposed method.

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Power (LFSR)</th>
<th>Power (LSA-TPG)</th>
<th>Percentage (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C432</td>
<td>1.6269</td>
<td>0.1887</td>
<td>11.6</td>
</tr>
<tr>
<td>C880</td>
<td>1.9172</td>
<td>0.1955</td>
<td>10.2</td>
</tr>
<tr>
<td>C3540</td>
<td>16.6386</td>
<td>1.3810</td>
<td>8.3</td>
</tr>
<tr>
<td>C5315</td>
<td>24.9804</td>
<td>1.6237</td>
<td>6.5</td>
</tr>
<tr>
<td>S298</td>
<td>4.8257</td>
<td>0.7576</td>
<td>15.7</td>
</tr>
<tr>
<td>S349</td>
<td>5.6920</td>
<td>0.9164</td>
<td>16.1</td>
</tr>
<tr>
<td>S386</td>
<td>2.1305</td>
<td>0.2407</td>
<td>11.3</td>
</tr>
<tr>
<td>S420</td>
<td>6.4563</td>
<td>0.5294</td>
<td>8.2</td>
</tr>
<tr>
<td>S526</td>
<td>6.6671</td>
<td>0.9867</td>
<td>14.8</td>
</tr>
<tr>
<td>S1238</td>
<td>10.7340</td>
<td>1.2237</td>
<td>11.4</td>
</tr>
<tr>
<td>S1488</td>
<td>10.6316</td>
<td>1.7967</td>
<td>16.9</td>
</tr>
<tr>
<td>S5378</td>
<td>51.8313</td>
<td>6.6344</td>
<td>12.8</td>
</tr>
</tbody>
</table>

In Table I, the column ‘Power(LFSR)’ refers to the average test power consumption with the traditional LFSR circuit. ‘Power (LSA-TPG)’ refers to the average test power consumption with the proposed method in this paper. Ratio is the result of power (LSA-TPG) and power (LFSR). It can be found that C5315 consumes 1.6237 mW test power with the method in this paper, while 24.9804 mW with the LFSR circuit. The ratio of the former to the latter is only 6.5%. For other benchmarks, this ratio is between 8.2% and 16.9%, and the average ratio is 11.98%, while the ratio in [4] is between 23.23% and 52.06%. Obviously, there are much more switching activities for multiple input changing sequence while single input changing sequence only change one bit in every clock, thus power consumption is greatly reduced. The results show that the proposed method can achieve better test power reduction than any previous low power methods.

Fig. 5 compares the power consumption between LFSR and the proposed structure LSA-TPG.
Fig. 5 shows that both combinational circuits and sequential circuits can achieve good power consumption reduction.

B. Fault Coverage

The results of fault simulation for ISCAS’89 benchmark circuits are shown in Table II. LFSR and LSA-TPG refer to the traditional LFSR, and proposed method in this paper respectively. Column ‘TL’, ‘FC’ refers to test vectors’ length and fault coverage respectively. ‘PI No.’ is the total number of the CUT’s primary inputs and pseudo primary inputs.

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>PI No.</th>
<th>LFSR TL</th>
<th>LFSR FC</th>
<th>LSA-TPG TL</th>
<th>LSA-TPG FC</th>
</tr>
</thead>
<tbody>
<tr>
<td>C432</td>
<td>36</td>
<td>2648</td>
<td>100</td>
<td>2648</td>
<td>100</td>
</tr>
<tr>
<td>C880</td>
<td>60</td>
<td>11920</td>
<td>100</td>
<td>11920</td>
<td>100</td>
</tr>
<tr>
<td>C3540</td>
<td>50</td>
<td>5168</td>
<td>98.36</td>
<td>5168</td>
<td>98.36</td>
</tr>
<tr>
<td>C5315</td>
<td>178</td>
<td>15960</td>
<td>99.42</td>
<td>15960</td>
<td>99.42</td>
</tr>
<tr>
<td>S298</td>
<td>17</td>
<td>1200</td>
<td>100</td>
<td>1200</td>
<td>100</td>
</tr>
<tr>
<td>S349</td>
<td>24</td>
<td>2120</td>
<td>100</td>
<td>2856</td>
<td>100</td>
</tr>
<tr>
<td>S386</td>
<td>13</td>
<td>3156</td>
<td>96.73</td>
<td>2680</td>
<td>96.58</td>
</tr>
<tr>
<td>S420</td>
<td>34</td>
<td>20480</td>
<td>90.46</td>
<td>17936</td>
<td>90.82</td>
</tr>
<tr>
<td>S526</td>
<td>34</td>
<td>10240</td>
<td>100</td>
<td>9824</td>
<td>100</td>
</tr>
<tr>
<td>S1238</td>
<td>32</td>
<td>21324</td>
<td>92.67</td>
<td>15864</td>
<td>93.32</td>
</tr>
<tr>
<td>S1488</td>
<td>14</td>
<td>4248</td>
<td>99.96</td>
<td>4064</td>
<td>99.87</td>
</tr>
<tr>
<td>S5378</td>
<td>214</td>
<td>30164</td>
<td>97.83</td>
<td>19872</td>
<td>98.48</td>
</tr>
</tbody>
</table>

Table II shows that the proposed method LSA-TPG can achieve nearly the same fault coverage at the same test length compared to that of LFSR for 12 benchmarks. The proposed method can achieve 100% stuck at fault coverage at the test length comparable to that of LFSR for five benchmark circuits (C432, C880, S298, S349, S526). For other benchmark circuits, the stuck at fault coverage is between 90% and 100%. It can also achieve high stuck-at fault coverage at shorter test length than LFSR’s for benchmark circuits (S386, S420, S526, S1238, S1488, S5378).

The proposed BIST structure is also implemented with Synopsys Design Compiler and the hardware overhead is very small.

V. Conclusion

An efficient low power BIST scheme has been proposed in this paper. This method uses a modified pseudo-random pattern generator to produce seeds and then operates with the single input changing generator and an exclusive-OR array, thus pseudo-random signal input changing sequences are generated, which greatly minimize circuit switching activities. The proposed approach can get low power consumption and has high fault coverage.

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References